Remarks/Arguments begin on page 2 of this paper.

Appendix including a sheet listing the status of the related patent applications is attached following page 10 of this paper.

REMARKS

The Examiner is thanked for the thorough examination and search of the subject.

Claims 55, 57, 58, 60-62 and 66-80 are pending; Claims 1-54, 56, 59 and 63-65 have been canceled. No new matter is believed to have been added.

The Appendix includes a sheet listing the status, updated to Jun. 17, 2009, of the related patent applications.

Response to Claim Rejections under 35 U.S.C. 103

Applicants respectfully traverse the rejections for at least the reasons set forth below.

Response to Claims 55 and 57, 58, 60-62 and 66-68

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As previously presented, independent Claim 55 is recited below:

55. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper,

multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to said second metal pad through an opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a titanium-containing layer between said second metal pad and said copper pillar, wherein said titanium-containing layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad;

a nickel-containing layer between said copper pillar and said solder metal; and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

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Reconsiderations of Claims 55, 57, 58, 60-62 and 66-68 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 55 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use a titanium containing layer in the invention of Nozawa because a titanium containing layer is conventionally known in the art layer used as barrier layer or a wetting/adhesion layer on a pad, as evinced by Farnworth, US Patent 5,851,911 (2, 28-44)." and that "it would have been obvious to one of ordinary skill in the

art at the time of the invention to use a nickel-containing layer in the invention of Nozawa because a nickel-containing layer is conventionally known in the art layer used as barrier layer or a wetting/adhesion layer, as evinced by Farnworth, US Patent 5,851,911 (2, 28-44)." ~ *See line 21 of page 4 through line 3 of page 5 and lines 6-11 on page 5, in the last Office Action mailed Mar. 23, 2009* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to apply Farnworth et al.'s titanium-containing or nickel-containing layer to Nozawa's metal bump. Nozawa's metal bump comprises a cylinder 122 having such a great height of at least 12 micrometers and a width dramatically smaller than a width of a solder bump 200, and surrounded by a resin 126. ~ *See Fig. 1 in U.S. Pat. No. 6,181,010* ~ However, Farnworth et al.'s metal bump does not comprise a cylinder having a great height and a small width, and surrounded by a resin. ~ *See Fig. 1h in U.S. Pat. No. 5,851,911* ~ The mechanical considerations for Nozawa's metal bump are significantly different from those for Farnworth et al.'s metal bump due to a design for a shrinking cylinder surrounded by a resin. Therefore, Farnworth et al.'s titanium-containing or nickel-containing layer is believed not to be readily applicable to Nozawa's metal bump.

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to

protect and strengthen the package, as evinced by Farnworth, US Patent 5,851,911 (2, 1-5)." ~ *See lines 15-18 on page 5, in the last Office Action mailed Mar. 23, 2009* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is usually used in a chip package with fine-pitched solder bumps to protect the solder bumps. ~ *See col. 2, lines 1-5 in U.S. Pat. No. 5,851,911* ~ However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill, formed between a chip and a substrate, enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 55 is respectfully requested.

Applicants respectfully submit independent Claim 55 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 57, 58, 60-62 and 67-68 patently define over the prior art as well.

Response to Claims 69-80

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As previously presented, independent Claim 69 is recited below:

69. A chip package comprising:

a substrate having a first side and a second side opposite to said first side, wherein said substrate comprises multiple contact points at said second side, a solder mask at said first side, an interconnect covered by said solder mask and a first metal pad comprising a region uncovered by said solder mask, wherein said first metal pad is connected to said interconnect;

a chip over said first side of said substrate, wherein said chip comprises a silicon substrate, multiple layers of interconnecting lines comprising copper, multiple insulating layers comprising an oxide material, multiple metal vias in said multiple insulating layers and between said multiple layers of interconnecting lines, wherein said multiple metal vias are connected to said multiple layers of interconnecting lines, and a polymer layer;

a copper pillar between said first metal pad and a second metal pad of said multiple layers of interconnecting lines, wherein said copper pillar is connected to said second metal pad through an opening in said polymer layer, and wherein said copper pillar has a thickness between 10 and 100 micrometers;

a metal layer between said second metal pad and said copper pillar, wherein said metal layer is on said second metal pad, on said polymer layer and in said opening in said polymer layer;

a solder metal between said copper pillar and said first metal pad, wherein said solder metal is connected to said first metal pad; and

an underfill between said chip and said first side of said substrate, wherein said underfill contacts with said chip and said first side of said substrate and encloses said copper pillar.

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Reconsiderations of Claims 69-80 rejected under 35 U.S.C. 103(a) as being unpatentable over Nozawa (U.S. Pat. No. 6,181,010) are requested based on the following remarks.

Applicants respectfully assert that the chip package claimed in Claim 69 patentably distinguishes over the citation by Nozawa (U.S. Pat. No. 6,181,010).

The Examiner considers that "it would have been obvious to one of ordinary skill in the art at the time of the invention to use an underfill between said semiconductor device and said substrate because underfills are commonly known used by skilled artisans to protect and strengthen the package, as evinced by Farnworth, US Patent 5,851,911 (2, 1-5)." ~ *See lines 15-18 on page 5, in the last Office Action mailed Mar. 23, 2009* ~

Applicants respectfully traverse the Examiner's opinion because it would have been unobvious to one of ordinary skill in the art at the time of the invention to use an underfill in the invention of Nozawa. Typically, a conventional underfill is usually used in a chip package with fine-pitched solder bumps to protect the solder bumps. ~ *See col. 2, lines 1-5 in U.S. Pat. No. 5,851,911* ~ However, Nozawa's connecting structure composed of elements 122, 124 and 200, having the metal pillar 122 to be protected by a polymer layer 126 before the bump 200 is connected to an external circuit, is significantly different from a conventional metal bump not protected by any polymer layer before the conventional metal bump is connected to an external circuit. Therefore, Nozawa's connecting structure 122, 124 and 200 could be achieved without any underfill, formed between a chip and a

substrate, enclosing Nozawa's connecting structure 122, 124 and 200, as shown in Fig. 9 in Nozawa's teaching, because a polymer layer 126 has been formed to protect the conducting layer 122 of Nozawa's connecting structure 122, 124 and 200 before Nozawa's bump 200 is connected to an external circuit. Therefore, the conventional underfill is believed to be unnecessary to be filled into a gap between a chip and a substrate in Nozawa's chip package.

For at least the foregoing reasons, withdrawal of the rejection under 35 U.S.C. 103(a) to Claim 69 is respectfully requested.

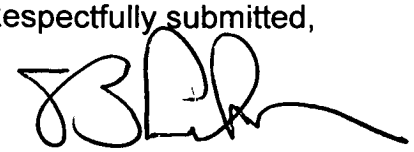
Applicants respectfully submit independent Claim 69 patently distinguishes over the prior art references, and should be allowed. For at least the same reasons, dependent claims 70-80 patently define over the prior art as well.

Conclusion

Some or all of the pending claims are believed to be in condition for allowance. Accordingly, allowance of the claims and the application as a whole are respectfully requested.

It is requested that should Examiner Zarneke not find that the Claims are now Allowable that he call the undersigned at 845 452-5863 to overcome any problems preventing allowance.

Respectfully submitted,



Stephen B. Ackerman, Reg. No. 37,761

Appendix: Sheet listing the status of the related patent applications

Appendix

Serial Number	Filing Date	Examiner Name	Status
11/389,717	3/27/2006	ZARNEKE, DAVID A	Non-Final office action mailed on 5/28/2009
11/981,138	10/31/2007	ZARNEKE, DAVID A	Non-Final office action mailed on 5/27/2009
11/981,125	10/31/2007	ZARNEKE, DAVID A	Non-Final office action mailed on 6/1/2009
12/384,977	4/9/2009		

Updated to 6/17/2009